

REMARKS

The Notice of Allowability provides that the drawings are objected to under 37 CFR 1.83(a) as failing to show every feature specified in the claims. In particular, the Notice of Allowability asserts that the feature of the gates being shorted together as covered in independent Claim 53 and the claims depending from Claim 53 must be shown in the drawings or the feature canceled from those claims. Instead of asserting that the allegedly non-shown feature must be canceled from Claim 53 and its dependent claims, the Examiner presumably means to assert that those claims must be canceled since canceling a non-shown feature from an allowed claim could impermissibly broaden the claim or could make it inoperative. The Notice of Allowability further provides that no new matter is to be entered.

Allowed Claim 53 is repeated below:

53. A structure comprising:

a plate region and a body region of a semiconductor body, the plate and body regions being of opposite conductivity types and meeting each other to form a p-n junction;

a gate dielectric layer situated over the semiconductor body and contacting the body region;

a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the gate electrode comprising multiple gate electrode portions of doped semiconductor material, the gate electrode portions being electrically shorted to one another, each gate electrode portion (a) being continuous with at least one other of the gate electrode portions and (b) being of different conductivity type or/and different average net dopant concentration than each other gate electrode portion.

Subject to the recited gate electrode portions comprising doped semiconductor material, being electrically shorted together, and being continuous with one another in the recited manner, Claim 53 requires that each gate electrode portion be (I) of different conductivity type than each other gate electrode portion or/and (II) of different average net dopant concentration than other gate electrode portion.

All of the structural features associated with the varactor structure of condition I of Claim 53 are illustrated in application Fig. 14 as verbally described in paragraphs 186 - 193 of the specification. The gate electrode portions recited in Claim 53 for condition I are implemented with n++ polycrystalline silicon ("polysilicon") lower gate electrode portion 112LA and p++ polysilicon lower gate electrode portion 112LB that meet to form pn junction 190 in Fig. 14. Metallic upper layer 112U in Fig. 14 electrically shorts lower gate

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

electrode portions 112LA and 112LB together. As a result, Fig. 14 satisfies the 37 CFR 1.83(a) illustration requirement for Claim 53 in connection with condition I.

Varactor structures that meet condition II of Claim 53 are verbally described in paragraphs 194 and 195 of the specification as variations of the varactor structure of Fig. 14. However, varactor structures meeting condition II of Claim 53 are not illustrated in the drawings as originally filed.

In order to satisfy the 37 CFR 1.83(a) illustration requirement for Claim 53 in connection with condition II, Figs. 14.1 and 14.2 are being added to the application's drawings via the accompanying Amendment to Drawings under 37 CFR 1.312. New Fig. 14.1 is a variation of Fig. 14 in which lower gate electrode portion 112LB is changed from p++ polysilicon to n++ polysilicon at a lower average net dopant concentration than the n++ polysilicon of lower gate electrode portion 112LA in accordance with specification paragraph 194. New Fig. 14.2 is a complementary variation of Fig. 14 in which lower gate electrode portion 112LA is changed from n++ polysilicon to p++ polysilicon at a lower average net dopant concentration than the p++ polysilicon of lower gate electrode portion 112LB likewise in accordance with specification paragraph 194. To emphasize that gate electrode portions 112LA and 112LB are of different polysilicon dopant concentrations in Figs. 14.1 and 14.2, portions 112LA and 112LB in each Fig. 14.1 or 14.2 are also respectively provided with the labels "N_{POLYA}" and "N_{POLYB}" representing the respective average net polysilicon dopant concentrations of portions 112LA and 112LB.

Polysilicon gate electrode portions 112LA and 112LB are of the same conductivity type in Figs. 14.1 and 14.2. That is, portions 112LA and 112LB are both n type in Fig. 14.1 and both p type in Fig. 14.2. Consequently, pn junction 190 of the varactor of Fig. 14 is not present in the varactor of Fig. 14.1 or 14.2.

The specification has been revised to accommodate Figs. 14.1 and 14.2 without introducing any new matter into the disclosure. In particular, paragraph 51 of the Brief-Description-of-the-Drawings section of the specification has been revised to specify that Figs. 14.1 and 14.2 are now part of the application.

Also, a pair of sentences have been inserted into paragraph 194 to respectively deal with Figs. 14.1 and 14.2. Using the reference notation "N_{POLYA}" and "N_{POLYB}" employed in Fig. 14.1, paragraph 194 now recites that "Such a variation of the varactor of Fig. 14 is

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

depicted in Fig. 14.1 where net polysilicon dopant concentration N_{POLYA} of n++ electrode portion 112LA exceeds net polysilicon dopant concentration N_{POLYB} of n++ electrode portion 112LB". This conforms with the earlier original statement, as corrected in the Amendment submitted 11 June 2004, that "If electrode portions 112LA and 112LB are both n-type and thus of opposite conductivity type to body region 100, electrode portion 112LA is doped more heavily n-type than is electrode portion 112LB".

Similarly using the reference notation " N_{POLYA} " and " N_{POLYB} " employed in Fig. 14.2, paragraph 194 now further recites that "Fig. 14.2 illustrates such a further variation of the varactor of Fig. 14 for which polysilicon dopant concentration N_{POLYA} of p++ electrode portion 112LA is less than polysilicon dopant concentration N_{POLYB} of p++ electrode portion 112LB". This insertion conforms with the earlier original statements, as corrected in the 11 June 2004 Amendment, that "The reverse dopant-concentration relationship arises if electrode portions 112LA and 112LB are both p-type and thus of the same conductivity type as body region 100" and "Per Eq. 33, electrode portion 112LA is doped more lightly p-type than is electrode portion 112LB".

The last sentence of paragraph 194, now split into two paragraphs, originally stated that "Since p-n junction 190 is absent in this variation, upper metallic gate electrode layer 112U can be deleted". In order to better accommodate the addition of Figs. 14.1 and 14.2, the last sentence of paragraph 194 has been revised to state that "Since p-n junction 190 is absent in the variations of Figs. 14.1 and 14.2, upper metallic gate electrode layer 112U can be deleted in such variations".

As the preceding comments indicate, the material illustrated in newly added Figs. 14.1 and 14.2 is disclosed in the application as filed. Aside from identifying Figs. 14.1 and 14.2, the specification revisions made to accommodate the addition of Figs. 14.1 and 14.2 are supported in the original specification. Accordingly, the addition of Figs. 14.1 and 14.2 and the associated revisions to the specification do not add new matter to the disclosure.

All of the structural features associated with the varactor structure of condition II of Claim 53 are illustrated in Figs. 14.1 and 14.2 as verbally described in specification paragraphs 194 and 195 in combination with specification paragraphs 186 - 193. The gate electrode portions recited in Claim 53 for condition II are implemented with n++ polysilicon lower gate electrode portions 112LA and 112LB in Fig. 14.1 and with p++ polysilicon lower

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
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Fax: 650-964-9779

gate electrode portions 112LA and 112LB in Fig. 14.2. Metallic upper layer 112U in each of Figs. 14.1 and 14.2 electrically shorts lower gate electrode portions 112LA and 112LB together. Hence, Figs. 14.1 and 14.2 satisfies the 37 CFR 1.83(a) illustration requirement for Claim 53 in connection with condition II.

As mentioned above, Fig. 14 satisfies the 37 CFR 1.83(a) illustration requirement for Claim 53 in connection with condition I. Consequently, the drawings now meet the requirement of 37 CFR 1.83(a) in connection with Claim 53 and its dependent claims that all of the structural features of the claims be illustrated in the drawings. The 37 CFR 1.83(a) objection to the drawings should be withdrawn.

Independent Claim 42, repeated below, includes conditions I and II of Claim 53:

42. A structure comprising:

a varactor comprising (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types and meeting each other to form a p-n junction, the gate electrode comprising multiple gate electrode portions of doped semiconductor material, each gate electrode portion being of different conductivity type or/and different average net dopant concentration than each other gate electrode portion; and

further electronic circuitry having a capacitance signal path for receiving the varactor to enable the further circuitry to perform an electronic function dependent on the varactor, the plate and body electrodes being situated in the capacitance signal path.

The addition of Figs. 14.1 and 14.2 enables the 37 CFR 1.83(a) illustration requirement to be met for Claim 42 and its dependent claims in the same way as in connection with Claim 53 and its dependent claims.

The claims were amended by the Examiner's Amendment in the Notice of Allowability as a result of a 11 October 2005 telephonic interview between the Examiner and Applicant's Attorney. The purpose of the Examiner's Amendment was to improve the clarity of the claims. However, the claim revisions made by the Examiner's Amendment do not fully correspond to what Applicant's Attorney agreed to in the 11 October 2005 telephonic interview.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

In the 11 October 2005 telephonic interview, Applicant's Attorney agreed to having the language "each gate dielectric portion extending to a location above the plate region or/and being continuous with a gate dielectric portion thinner than that gate dielectric portion" in independent Claim 34 changed to "each particular gate dielectric portion extending to a location above the plate region or/and being continuous with another a gate dielectric portion thinner than that particular gate dielectric portion" where underlining and strikethrough are respectively used to indicate added and deleted material. Instead, this language was instead changed to "a ~~each~~ particular gate dielectric portion extending to a location above the plate region or/and being continuous with another a gate dielectric layer ~~portion~~ thinner than the ~~that~~ particular gate dielectric portion" in the Examiner's Amendment.

Applicant's Attorney similarly agreed in the 11 October 2005 telephonic interview to having the language "each surface depletion portion meeting the plate region or/and being continuous with a surface depletion portion more lightly doped than that surface depletion portion" in independent Claim 39 changed to "each particular surface depletion portion meeting the plate region or/and being continuous with another a surface depletion portion more lightly doped than that particular surface depletion portion". This language in Claim 39 was instead changed to "a ~~each~~ particular surface depletion portion meeting the plate region or/and being continuous with another a surface depletion portion more lightly doped than the ~~that~~ particular surface depletion portion" in the Examiner's Amendment.

In the 11 October 2005 telephonic interview, Applicant's Attorney agreed to having the language "each inversion portion meeting the plate region or/and being continuous with another inversion portion whose zero-point threshold voltage is of lower magnitude than the zero-point threshold voltage of that inversion portion" in independent Claim 1 changed to "each particular inversion portion meeting the plate region or/and being continuous with another inversion portion whose zero-point threshold voltage is of lower magnitude than the zero-point threshold voltage of that particular inversion portion". However, this language in Claim 1 was not changed at all in the Examiner's Amendment.

Claims 1, 34, and 39 have been amended here so that their revised wording corresponds identically to what Applicant's Attorney agreed to in the 11 October 2005 telephonic interview. The scope of Claims 1, 34, and 39, as amended here, is the same as that existing prior to the Examiner's Amendment.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869

Tel.: 650-964-9767
Fax: 650-964-9779

Only independent Claims 1, 34, and 39 were dealt with in the 11 October 2005 telephonic interview. However, dependent Claims 7 and 11 are worded in the same way as the independent claim language that was revised as a result of the 11 October 2005 interview to improve the claim clarity. Accordingly, dependent Claims 7 and 11 have been amended here in the same manner as independent Claims 1, 34, and 39 so as to improve the clarity of Claims 7 and 11. The revisions to Claims 7 and 11 do not change their scope.

Finally, dependent Claim 41 introduces "a surface depletion region" identical to the surface depletion recited in independent Claim 39 from which Claim 41 depends. Inasmuch as the surface depletion region introduced into Claim 41 is redundant with that recited in Claim 39, Claim 41 has been amended to delete the redundant surface depletion region.

Entry of the present amendment and the accompanying Amendment to Drawings will not entail materially added work on the Examiner's part. No more than a cursory review of the record will be needed. Accordingly, this amendment and the Amendment to Drawings should be entered.

Please telephone Applicant's Attorney at 650-964-9767 if there are any questions.

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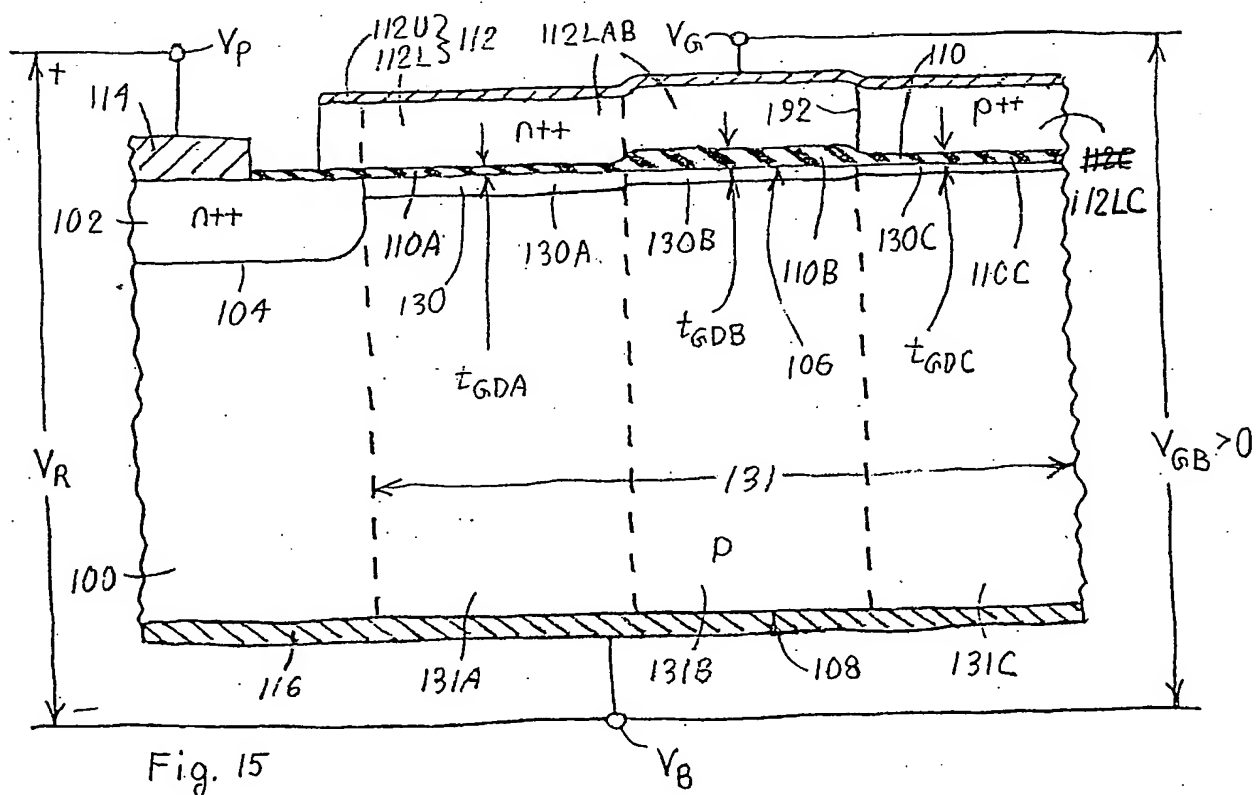
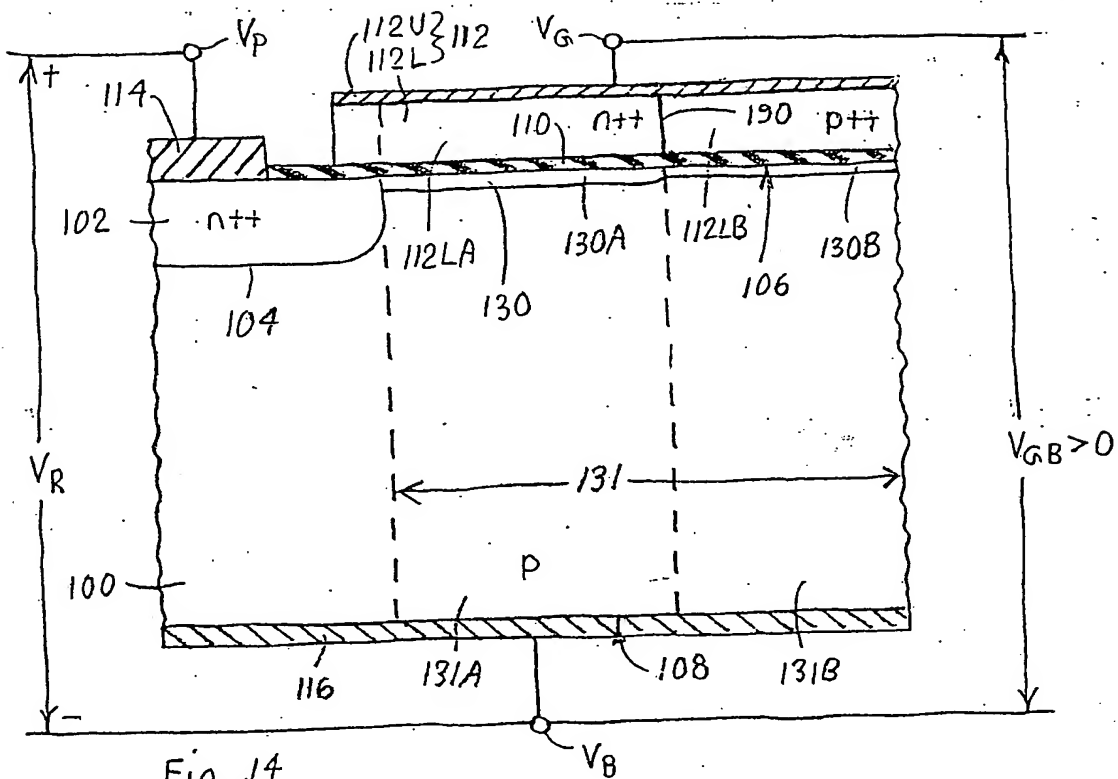
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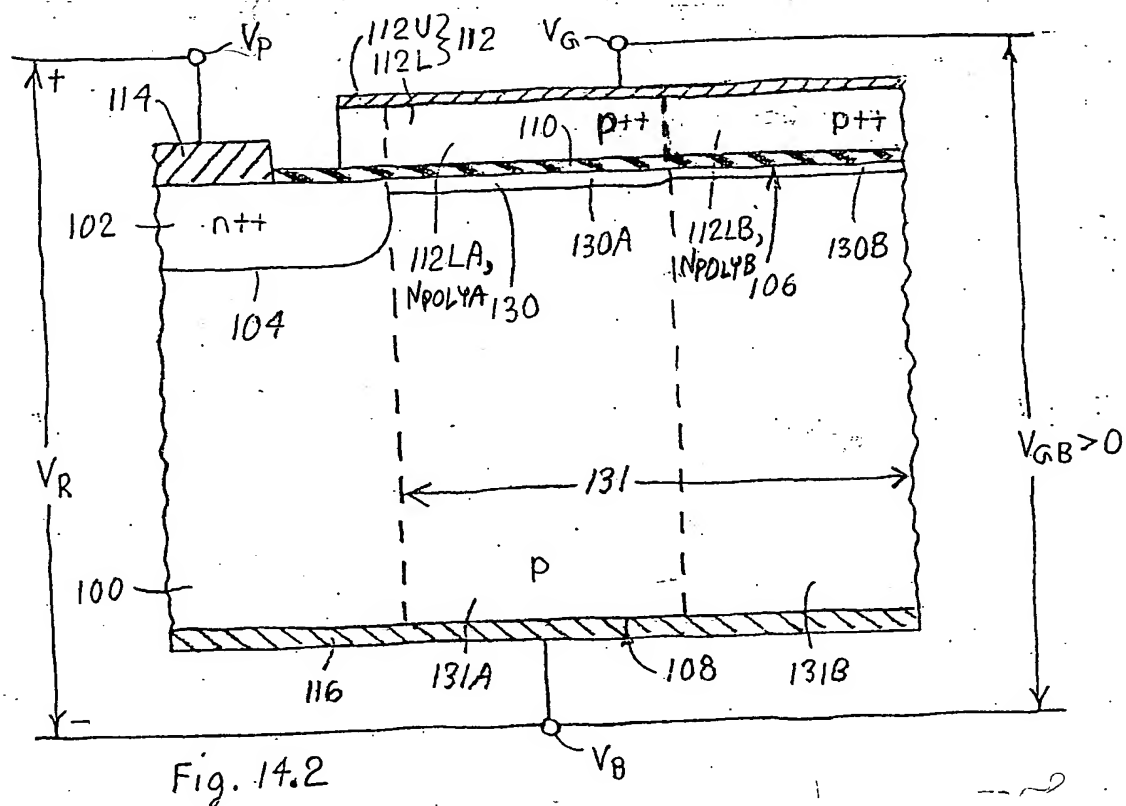
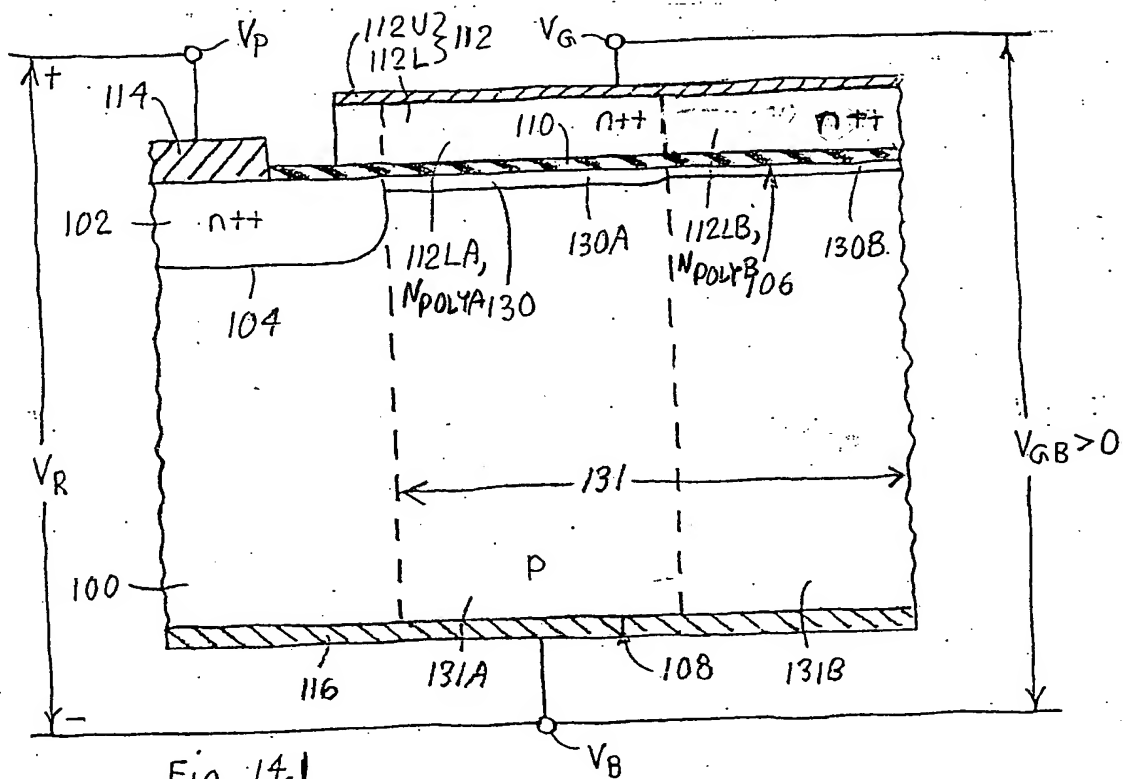


Ronald J. Meetin
Attorney for Applicant(s)
Reg. No. 29,089

210 Central Avenue
Mountain View, CA 94043-4869

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779





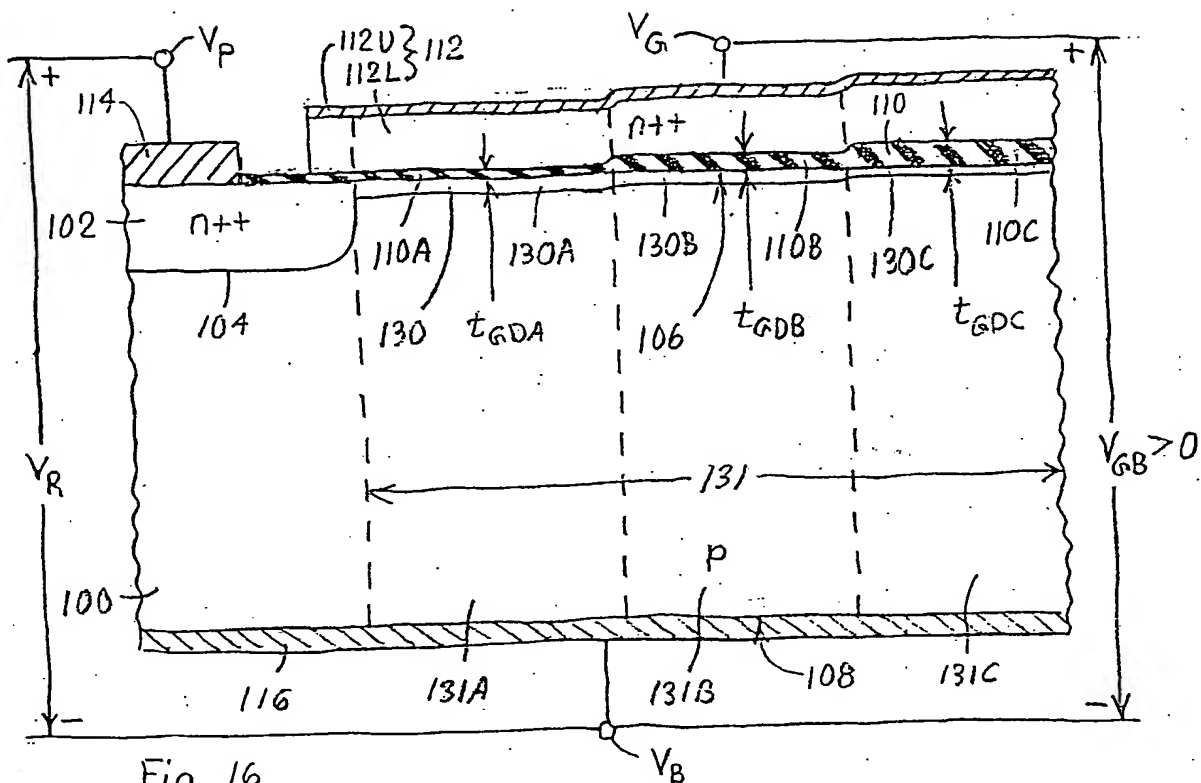


Fig. 16

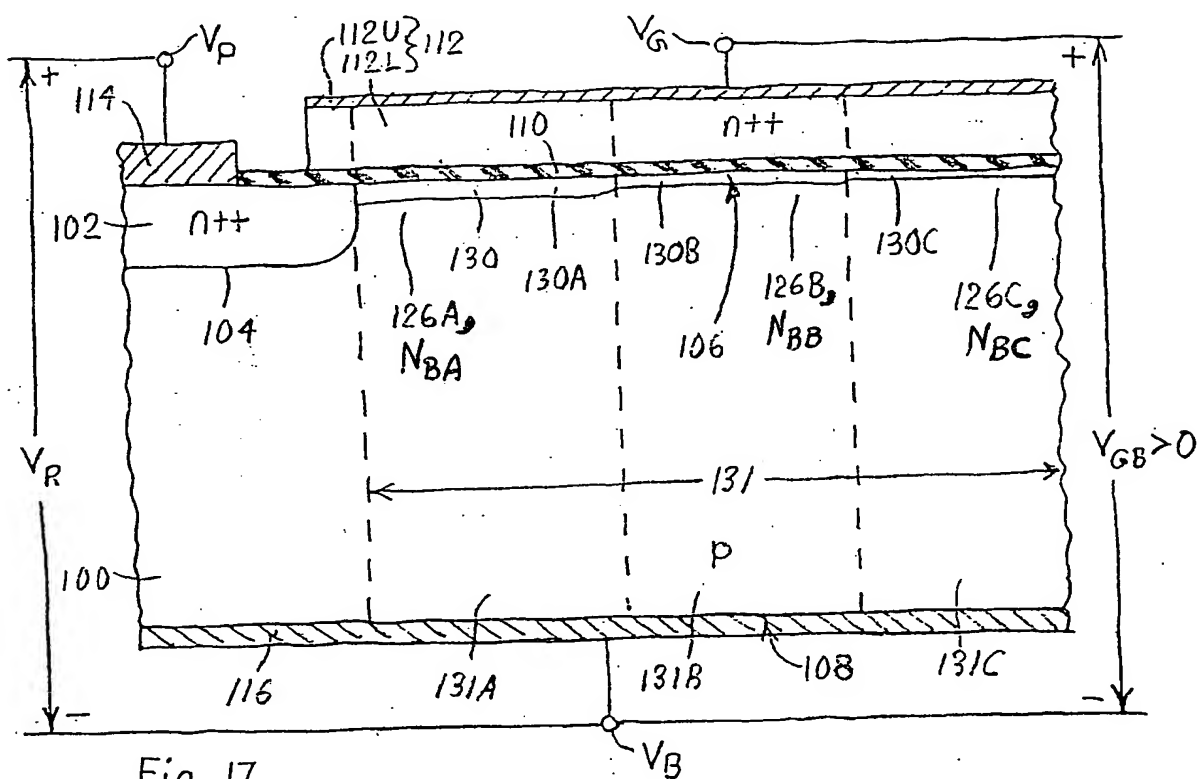


Fig. 17